PRELIMINARY

MOSTEK®

Z80 MICROCOMPUTER PERIPHERALS

Serial Timer Interrupt Controller

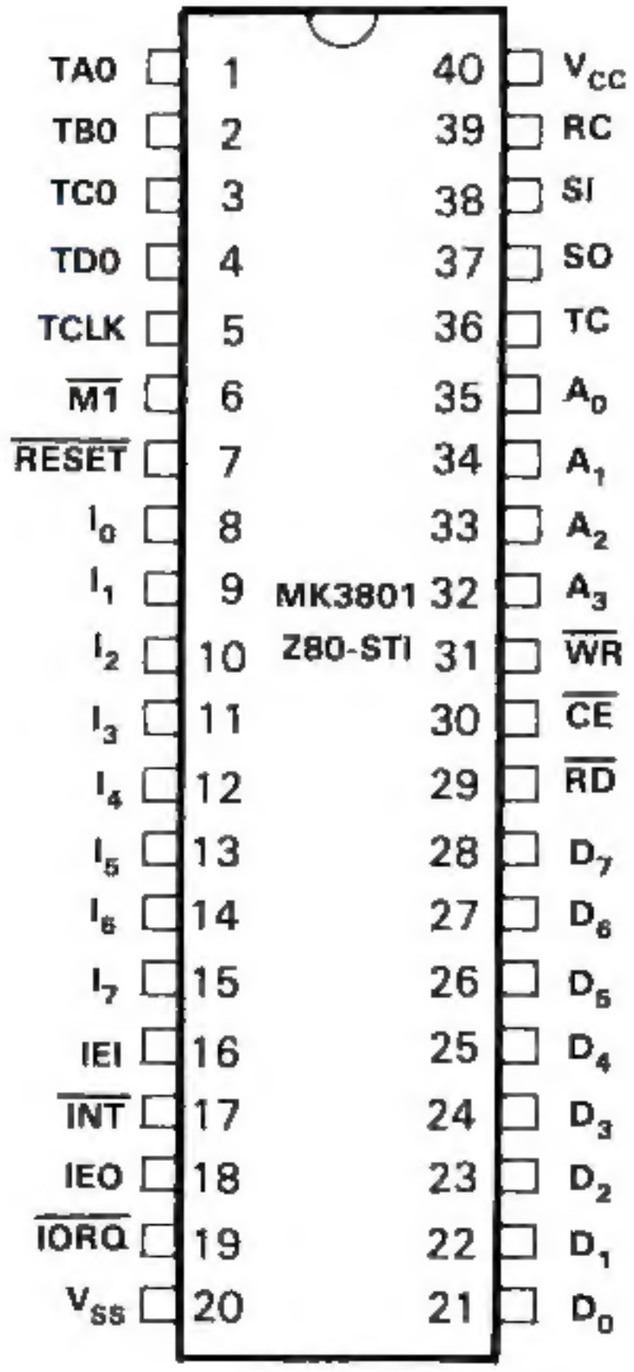
MK3801

FEATURES

- ☐ Full duplex USART with programmable DMA control signals
- ☐ Two binary delay timers
- ☐ Two full feature timers with
  - Delay to interrupt mode
  - Pulse width measurement mode
  - Event counter mode
- ☐ Eight general purpose lines with
  - Full bi-directional I/O capability
  - Edge triggered interrupts on either edge
- ☐ Full control of each interrupt channel
  - Enable/disable
  - Maskable
  - Automatic end-of-interrupt mode
  - Software end-of-interrupt mode
- ☐ 2.5 and 4 MHz versions available now, with 6 MHz version to follow

DEVICE PINOUT

Figure 1



INTRODUCTION

The MK3801 Z80 STI (Serial Timer Interrupt) is a multifunctional peripheral device for use in Z80 microprocessor based systems. It is designed to optimize current systems by reducing chip count and system costs. By providing a USART, four timers (two binary and two full function), and eight bi-directional I/O lines with individually programmable interrupts, the MK3801 can make substantial improvement to any Z80 based system.

Control and operation of the MK3801 are provided by 24 internal registers accessible by the Z80 bus. Sixteen of these registers are directly addressable and accessible; eight are indirectly addressable. Two of the four timers provide full service features, while the other two provide delay timer features only. Serial Communication is provided by the USART, which is capable of either asynchronous or synchronous operation, optional sync word recognition and stripping, and programmable DMA control handshake lines. Eight bi-directional I/O lines provide parallel I/O capability and individually programmable interrupt capability. The interrupt structure of the device is fully programmable for all interrupts, provides for interrupt vector generation, conforms to the Z80 daisy chain interrupt priority scheme, and supports automatic end of interrupt functions for the Z80.

SIGNAL NAME	DESCRIPTION
V_{SS}	Ground
V_{CC}	+5 volts (± 5 percent)
$\overline{CE}$	Chip Enable (Input, active low)
$\overline{RD}$	Read Enable (Input, active low)
$\overline{WR}$	Write Enable (Input, active low)
A_0-A_3	Address Inputs. Used to address one of the internal registers during a read or write operation
D_0-D_7	Data Bus (bi-directional)
$\overline{RESET}$	Device Reset (negative true). When activated, all internal registers (except for Timer or USART Data registers) will be cleared, all timers stopped, USART turned off, all interrupts disabled and all pending interrupts cleared, and all I/O lines placed in tri-state input mode.
I_0-I_7	General purpose I/O and interrupt lines
$\overline{INT}$	Interrupt Request (Output, active low, open drain)
$\overline{IORQ}$	Input/Output Request from Z80-CPU (input, active low). The $\overline{IORQ}$ signal is used in conjunction with $\overline{M1}$ to signal the MK3801 that the CPU is acknowledging its interrupt.
IEI	Interrupt Enable In, active High
IEO	Interrupt Enable Out, active High
SO	Serial Output
SI	Serial Input
RC	Receiver Clock Input
TC	Transmit Clock Input
TAO-TDO	Timer Outputs
TCLK	Timer Clock Input
$\overline{M1}$	Z80 Machine Cycle One (negative true)

PIN DESCRIPTION

Figure 1 illustrates the pinout of the MK3801. The functions of these individual pins are described above.

INTERNAL ORGANIZATION

Figure 2 illustrates the MK3801 internal organization, which supports the full set of timing, communications, parallel I/O, and interrupt processing functions available in the device.

CPU BUS I/O

The CPU BUS I/O provides the means of communications between the system and the MK3801. Data, Status, and Control Registers in the MK3801 are accessed by the bus in order to establish device parameters, assert control, and transfer status and data between the system and the MK3801.

Each register in the MK3801 is addressed over the address bus in conjunction with Chip Enable ($\overline{CE}$), while data is transferred over the eight bit Data bus under control of Read ($\overline{RD}$) and Write ($\overline{WR}$) signals.

REGISTER ACCESSES

All register accesses are independent of any system clock. To read a register, both $\overline{CE}$ and $\overline{RD}$ must be active. The internal read control signal is essentially the combination of both $\overline{CE}$ and $\overline{RD}$ active; thus the read operation will begin when the later of these two signals goes active and will end when the first signal goes inactive. The address bus must be stable prior to the start of the operation and must remain stable until the end of the operation. Unless a read operation or an interrupt acknowledge cycle is in progress, the data bus (D_0-D_7) will remain in the tri-state condition.

To write a register, both $\overline{CE}$ and $\overline{WR}$ must be active. The address must be stable prior to the start of the operation and must remain stable until the end of the operation. The data must be stable prior to the end of the operation and must remain stable until the end of the operation. The data presented on the bus will be latched into the register shortly after either $\overline{WR}$ or $\overline{CE}$ goes inactive.

INTERNAL REGISTERS

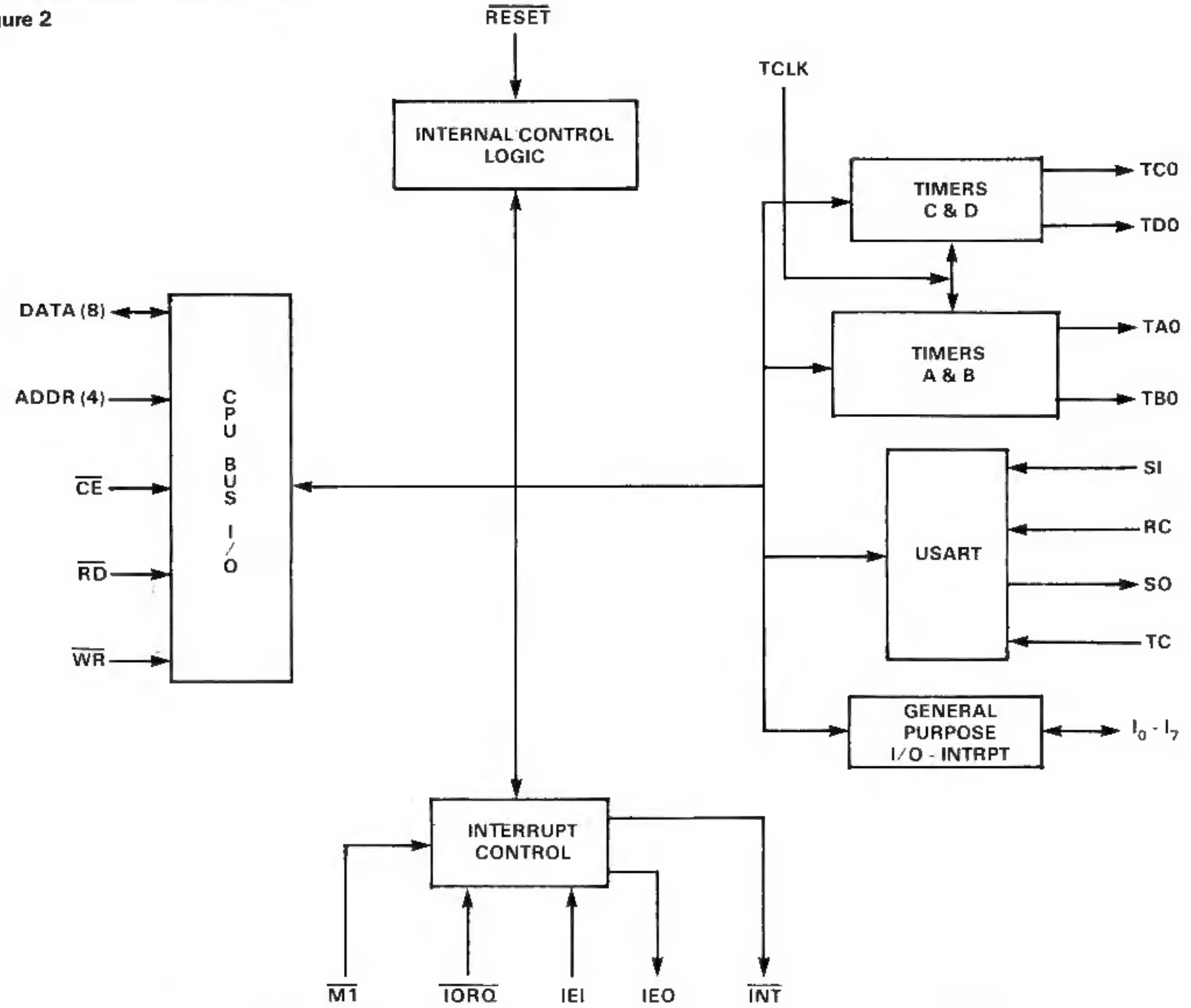
There are 24 internal registers used to control the operation of the STI. Sixteen of these registers are directly addressable and accessible. Eight registers are indirectly addressable via the Pointer/Vector Register and accessible via the Indirect Data Register.

DIRECTLY ADDRESSABLE REGISTERS

The Directly Addressable Registers are accessed by placing the address of the desired register on the address lines (A_0-A_3) during a write or read cycle. Figure 3 lists the Directly Addressable Registers.

INTERNAL ORGANIZATION

Figure 2



DIRECTLY ACCESSIBLE REGISTERS

Figure 3

ADDRESS	ABBREVIATION	REGISTER NAME
0	IDR	Indirect Data Register
1	GPIP	General Purpose I/O-Interrupt
2	IPRB	Interrupt Pending Register B
3	IPRA	Interrupt Pending Register A
4	ISRB	Interrupt in-Service Register B
5	ISRA	Interrupt in-Service Register A
6	IMRB	Interrupt Mask Register B
7	IMRA	Interrupt Mask Register A
8	PVR	Pointer/Vector Register
9	TABCR	Timers A and B Control Register

DIRECTLY ACCESSIBLE REGISTERS (Continued)
Figure 3

ADDRESS	ABBREVIATION	REGISTER NAME
A	TBDR	Timer B Data Register
B	TADR	Timer A Data Register
C	UCR	USART Control Register
D	RSR	Receiver Status Register
E	TSR	Transmitter Status Register
F	UDR	USART Data Register

INDIRECTLY ADDRESSABLE REGISTERS
Figure 4

INDIRECT ADDRESS	ABBREVIATION	REGISTER NAME
0	SCR	Sync Character Register
1	TDDR	Timer D Data Register
2	TCDR	Timer C Data Register
3	AER	Active Edge Register
4	IERB	Interrupt Enable Register B
5	IERA	Interrupt Enable Register A
6	DDR	Data Direction Register
7	TCDCR	Timers C and D Control Register

INDIRECTLY ADDRESSABLE REGISTERS

Indirectly Addressable Registers are addressed by placing the indirect address in bits IA0-IA2 of the Pointer/Vector Register, as defined in Figure 5. Data may be written to or read from the register indicated by these Indirect Register Address bits by a write or read access of the Indirect Data Register (selected when A_0-A_3 are all zero). The indirect address bits of the Pointer/Vector Register will remain unchanged after an indirect access. Repeated accesses of the Indirect Data Register will access the same indirect register as long as the indirect address in the Pointer/Vector Register remains unchanged. The Indirectly Addressable Registers are listed in Figure 4.

INTERRUPT VECTOR DEFINITION

Each individual function in the MK3801 is provided with a unique interrupt vector that is presented to the system during the interrupt acknowledge cycle. The interrupt vector returned during interrupt acknowledge is formed as shown in Figure 6. There are 16 vector addresses generated internally by the MK3801, one for each of the 16 interrupt channels. The three most significant bits of these vector addresses correspond to the three most significant bits of the Pointer/Vector Register shown in Figure 5. The least significant bit of each vector address is always 0, thus producing even vector addresses. The remaining 4 bits (IV_1 through IV_4) identify each of the 16 interrupt channels individually. The lowest priority channel responds with 0000 for IV_4-IV_1 respectively. The next higher priority channel responds with 0001, and so on in binary order, with the highest priority channel responding with 1111. Figure 7 lists each of the 16 interrupt channels in order of descending priority.

INTERRUPT CONTROL REGISTERS

The Interrupt Control Registers provide control of interrupt processing for all I/O facilities of the MK3801. These registers allow the programmer to enable or disable any or all of the 16 interrupts, provide masking for any interrupts, and access to the pending or in-service status of the interrupts. Optional End-of-Interrupt modes are available under software control. The format of each of the Interrupt Control Registers is presented in Figure 8.

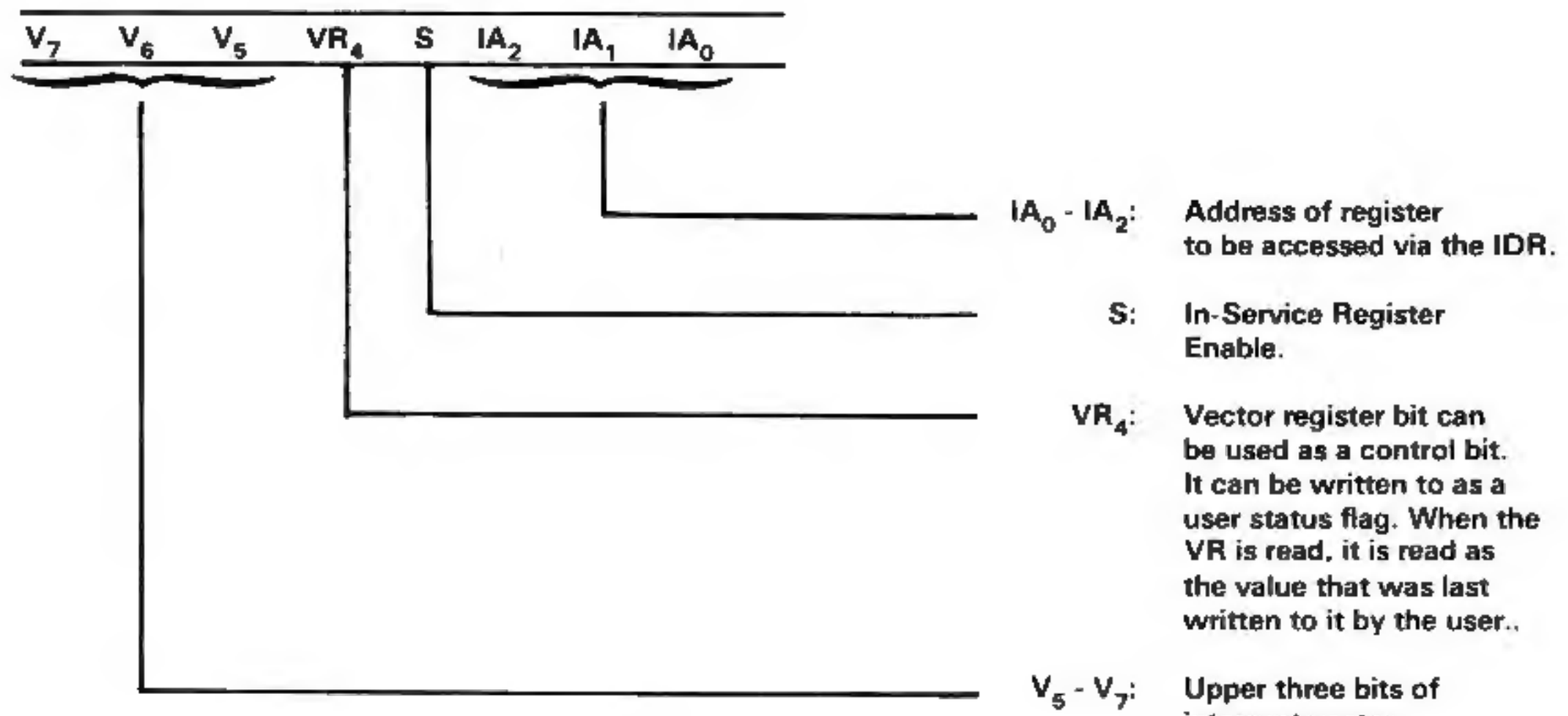
INTERRUPT OPERATION

The Interrupt Enable Registers enable or disable the setting of an interrupt in the Interrupt Pending Registers. A 0 in a bit of the Interrupt Enable Registers disables the interrupt for the associated channel while a 1 enables the interrupt.

Once an interrupt is enabled, the occurrence of an interrupting condition on that channel will cause the

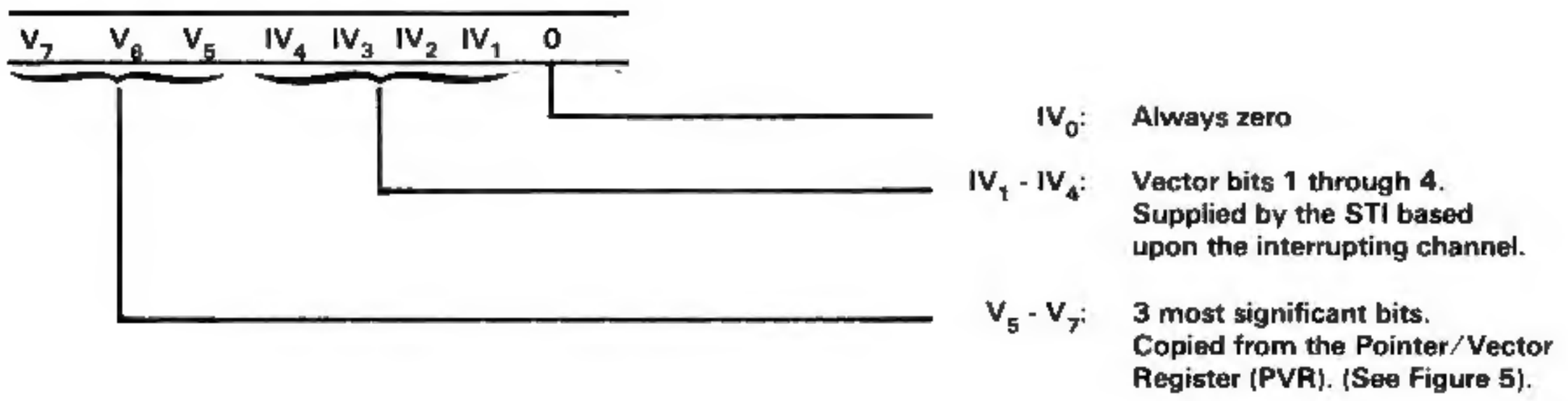
POINTER/VECTOR REGISTER (PVR) Port 08

Figure 5


V7 V6 V5 VR4 S IA2 IA1 IA0
IA0 - IA2: Address of register to be accessed via the IDR.
S: In-Service Register Enable.
VR4: Vector register bit can be used as a control bit. It can be written to as a user status flag. When the VR is read, it is read as the value that was last written to it by the user..
V5 - V7: Upper three bits of interrupt vector. Written into the VR by the user.

INTERRUPT VECTOR

Figure 6


V7 V6 V5 IV4 IV3 IV2 IV1 0
IV0: Always zero
IV1 - IV4: Vector bits 1 through 4. Supplied by the STI based upon the interrupting channel.
V5 - V7: 3 most significant bits. Copied from the Pointer/Vector Register (PVR). (See Figure 5).

corresponding bit in the Interrupt Pending Register to be set. This indicates that an interrupt is pending in the MK3801.

Pending interrupts are presented to the Z80 CPU in order of priority (see Figure 1) unless they have been masked off. This is done by clearing the bit in the Interrupt Mask Register corresponding to the channel whose interrupt is to be masked. The channel's interrupt will remain pending until the mask bit for that channel is set, at which time the interrupt for that channel will be processsed in order of priority.

When an interrupt vector is generated for a pending interrupt and passed to the Z80 CPU, the bit in the Interrupt Pending Register, associated with the channel generating the interrupt, will be cleared. At this time, no history of the interrupt remains in the MK3801.

In order to retain historical evidence of an interrupt being serviced by the Z80, the In-Service Register may be enabled by setting the S-bit in the Pointer/Vector Register (see Figure 5). If the In-Service Register is enabled, the bit of the In-Service Register corresponding to the interrupting channel will be set when the interrupt vector is passed to the Z80. At the same time, the Interrupt Pending bit will be cleared since the interrupt is now in service. The In-Service bit will be cleared on execution of a Return-from-Interrupt (H'ED4D') instruction. The In-Service Registers are directly addressable, and the In-Service bit for any interrupt may be cleared by writing to the In-Service Register if the Return-from-Interrupt instruction is not used.

INTERRUPT CONTROL REGISTER DEFINITIONS

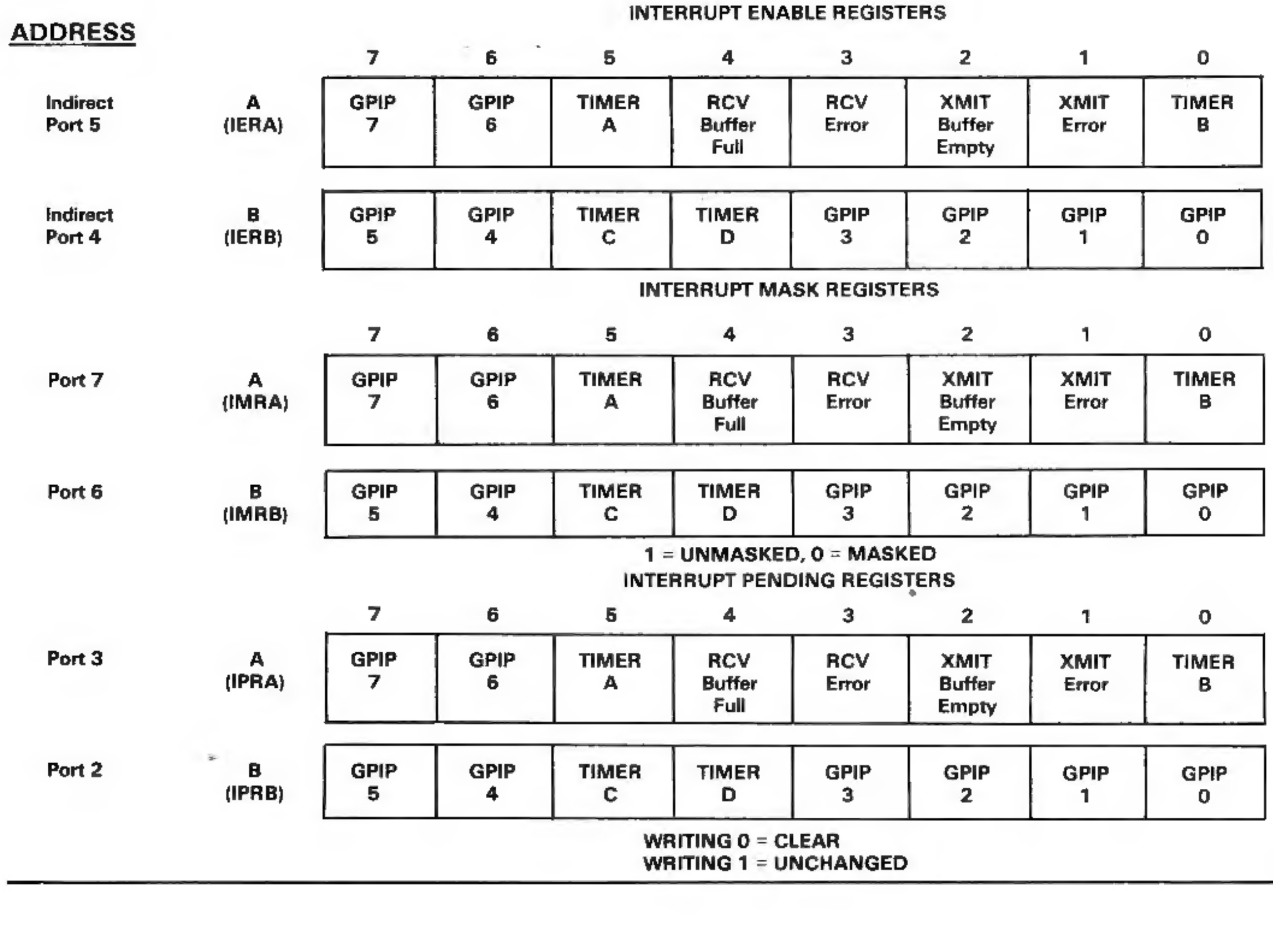
Figure 7

There are sixteen interrupt channels on the STI arranged in the following priority:

PRIORITY	CHANNEL	DESCRIPTION	ALTERNATE USAGE
HIGHEST	1111	General Purpose Interrupt 7 (I_7)	
	1110	General Purpose Interrupt 6 (I_6)	
	1101	Timer A	
	1100	Receive Buffer Full	
	1011	Receive Error	
	1010	Transmit Buffer Empty	
	1001	Transmit Error	
	1000	Timer B	
	0111	General Purpose Interrupt 5 (I_5)	
	0110	General Purpose Interrupt 4 (I_4)	TA (PW-Event)
	0101	Timer C	
	0100	Timer D	
	0011	General Purpose Interrupt 3 (I_3)	TB (PW-Event)
	0010	General Purpose Interrupt 2 (I_2)	
	0001	General Purpose Interrupt 1 (I_1)	DMA (TR)TX
LOWEST	0000	General Purpose Interrupt 0 (I_0)	DMA (RR)REC

INTERRUPT CONTROL REGISTERS

Figure 8



INTERRUPT CONTROL REGISTERS (Continued)

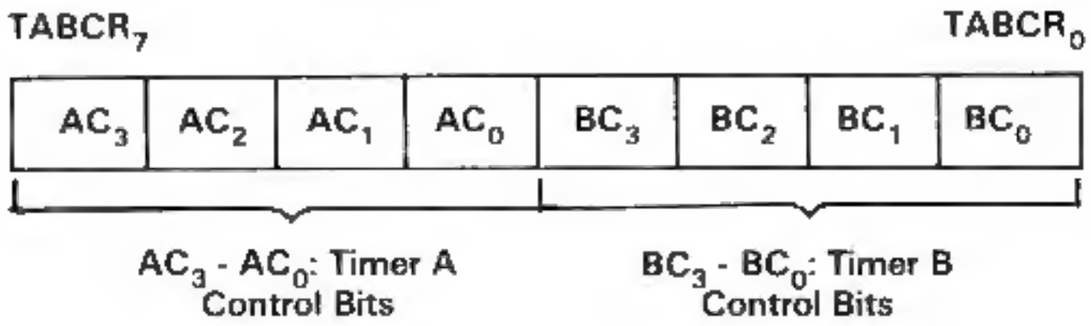
Figure 8

INTERRUPT SERVICE REGISTERS

ADDRESS		7	6	5	4	3	2	1	0
Port 5	A (ISRA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	TIMER B
Port 4	B (ISRB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

TIMER A and B CONTROL REGISTER (TABCR) Port 9

Figure 9



The four control bits are used to select the timer mode and prescale value, as follows:

CONTROL BIT DEFINITION

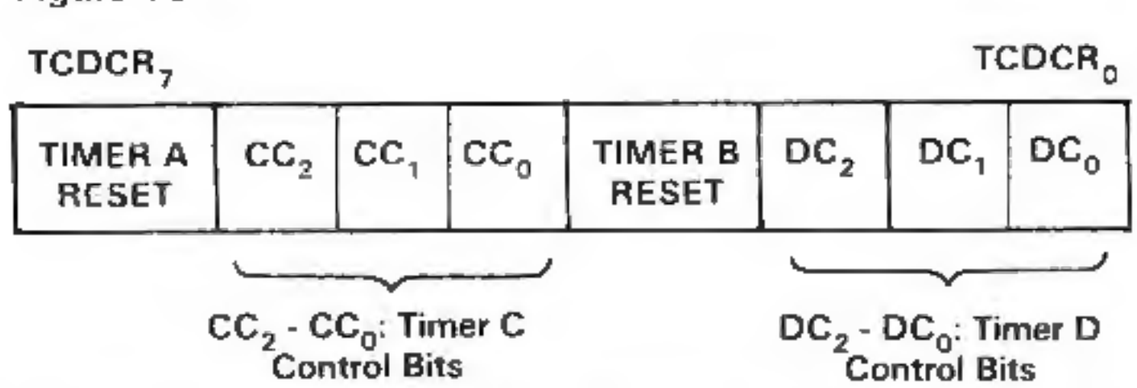
C_3	C_2	C_1	C_0	
0	0	0	0	Timer Stopped
0	0	0	1	Delay Mode, ÷4 Prescale
0	0	1	0	Delay Mode, ÷10 Prescale
0	0	1	1	Delay Mode, ÷16 Prescale
0	1	0	0	Delay Mode, ÷50 Prescale
0	1	0	1	Delay Mode, ÷64 Prescale
0	1	1	0	Delay Mode, ÷100 Prescale
0	1	1	1	Delay Mode, ÷200 Prescale
1	0	0	0	Event Count Mode
1	0	0	1	Pulse Width Mode, ÷4 Prescale
1	0	1	0	Pulse Width Mode, ÷10 Prescale
1	0	1	1	Pulse Width Mode, ÷16 Prescale
1	1	0	0	Pulse Width Mode, ÷50 Prescale
1	1	0	1	Pulse Width Mode, ÷64 Prescale
1	1	1	0	Pulse Width Mode, ÷100 Prescale
1	1	1	1	Pulse Width Mode, ÷200 Prescale

TIMER A DATA REGISTER AND TIMER B DATA REGISTER (TADR, TBDR) Port B & Port A

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

TIMER C and D CONTROL REGISTER (TCDCR) Indirect Port 7

Figure 10



Three control bits are used to control each timer, as defined below:

CONTROL BIT DEFINITION

C_2	C_1	C_0	
0	0	0	Timer Stopped
0	0	1	Delay Mode, ÷4 Prescale
0	1	0	Delay Mode, ÷10 Prescale
0	1	1	Delay Mode, ÷16 Prescale
1	0	0	Delay Mode, ÷50 Prescale
1	0	1	Delay Mode, ÷64 Prescale
1	1	0	Delay Mode, ÷100 Prescale
1	1	1	Delay Mode, ÷200 Prescale

TIMER C DATA REGISTER and TIMER D DATA REGISTER (TCDR, TDDR) Indirect, Port 2 and Indirect Port 1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

TIMERS

Four timers are available on the MK3801. Two provide full service features including delay timer operation, event counter operation, pulse width measurement operation, and pulse generation. The two other timers provide delay timer features only, and may be used for baud rate generators for use with the USART.

All timers are prescaler/counter timers, with a common independent clock input, and are not required to be operated from the system clock. In addition, all timers have a time-out output function that toggles each time the timer times out.

TIMER CONTROL REGISTERS

The 4 timers (A,B,C, and D) are programmed via 2 control registers and 4 timer data registers. Timers A and B are controlled by a single register (TABCR) and two timer data registers (TADR,TBDR). Timers C and D are controlled by a second control register (TCDCR) and two timer data

registers (TCDR, TDDR). Bits in the control registers allow the selection of operational mode, prescale, and control, while the data registers are used to read the timer or write the time constant register. General Purpose I/O Interrupt pins 3 (TB) and 4 (TA) are used for timer B and A inputs in event and pulse width modes. Figure 9 illustrates the Control and Data Register for timers A and B, while Figure 10 illustrates the Control and Data registers for timers C and D.

USART

Serial Communication is provided by the USART, which is capable of either asynchronous or synchronous operation. Variable word width and start/stop bit configurations are available under software control for asynchronous operation. For synchronous operation, a Sync Word is provided to establish synchronization during receive operations. The Sync Word will also be repeatedly transmitted when no other data is available for transmission. Operational modes exist to allow stripping of all Sync Words received in synchronous operation, and to allow the operation of DMA control handshake lines by the USART through General Purpose I/O Port lines 0 and 1. Separate receive and transmit clocks are available, and separate receive and transmit status and data bytes allow independent operation of the transmit and receive sections.

USART CONTROL REGISTERS

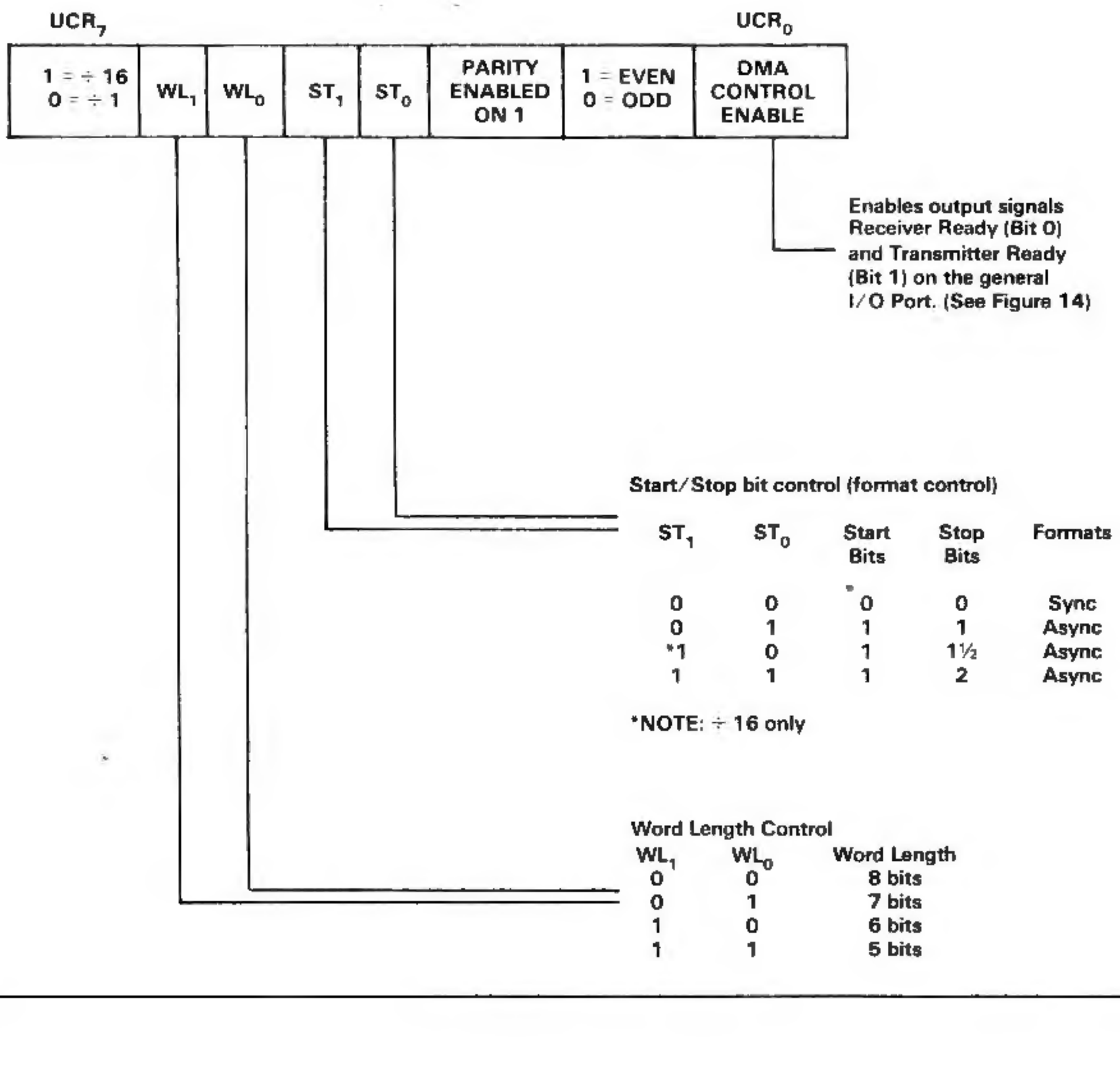
The USART is provided with 3 control/status registers and a data register. The programmer may specify operational parameters for the USART via the Control Register, as shown in Figure 11. Status of both the Receiver and Transmitter sections is accessed by means of the 2 Status Registers, as shown in Figure 12. Data written to the Data Register is passed to the transmitter, while reading the data register will access data received by the USART. The USART Data Register form is illustrated in Figure 13.

ERROR CONDITIONS

Error conditions in the USART are determined by monitoring the Receive Status Register (Port D) and the Transmitter Status Register (Port E). These error conditions are only valid for each word boundary and are not latched. When executing block transfers of data, it is necessary to save any errors so that they can be checked at the end of a block. In order to save error conditions during data transfer, the STI interrupt controller may be used by enabling error

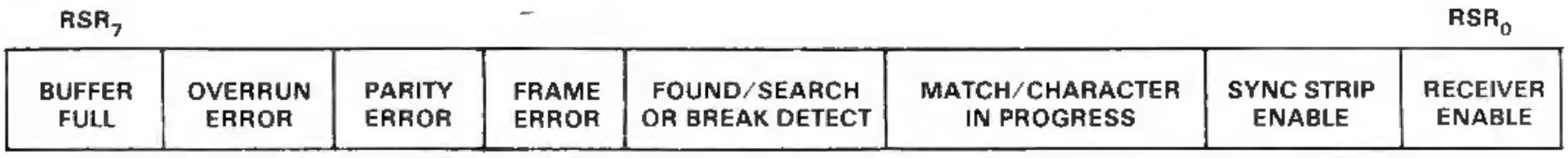
USART CONTROL REGISTER (UCR) Port C

Figure 11


UCR7
UCR0
1 = ÷ 16
0 = ÷ 1
WL1
WL0
ST1
ST0
PARITY ENABLED ON 1
1 = EVEN
0 = ODD
DMA CONTROL ENABLE
Enables output signals Receiver Ready (Bit 0) and Transmitter Ready (Bit 1) on the general I/O Port. (See Figure 14)
Start/Stop bit control (format control)
ST1 ST0 Start Bits Stop Bits Formats
0 0 0 0 Sync
0 1 1 1 Async
*1 0 1 1½ Async
1 1 1 2 Async
*NOTE: ÷ 16 only
Word Length Control
WL1 WL0 Word Length
0 0 8 bits
0 1 7 bits
1 0 6 bits
1 1 5 bits

RECEIVER STATUS REGISTER (RSR) Port D

Figure 12



TRANSMITTER STATUS REGISTER (TSR) Port E

H	L	Serial Output State
0	0	Hi-Z
0	1	Low ("0")
1	0	High
1	1	Loop*

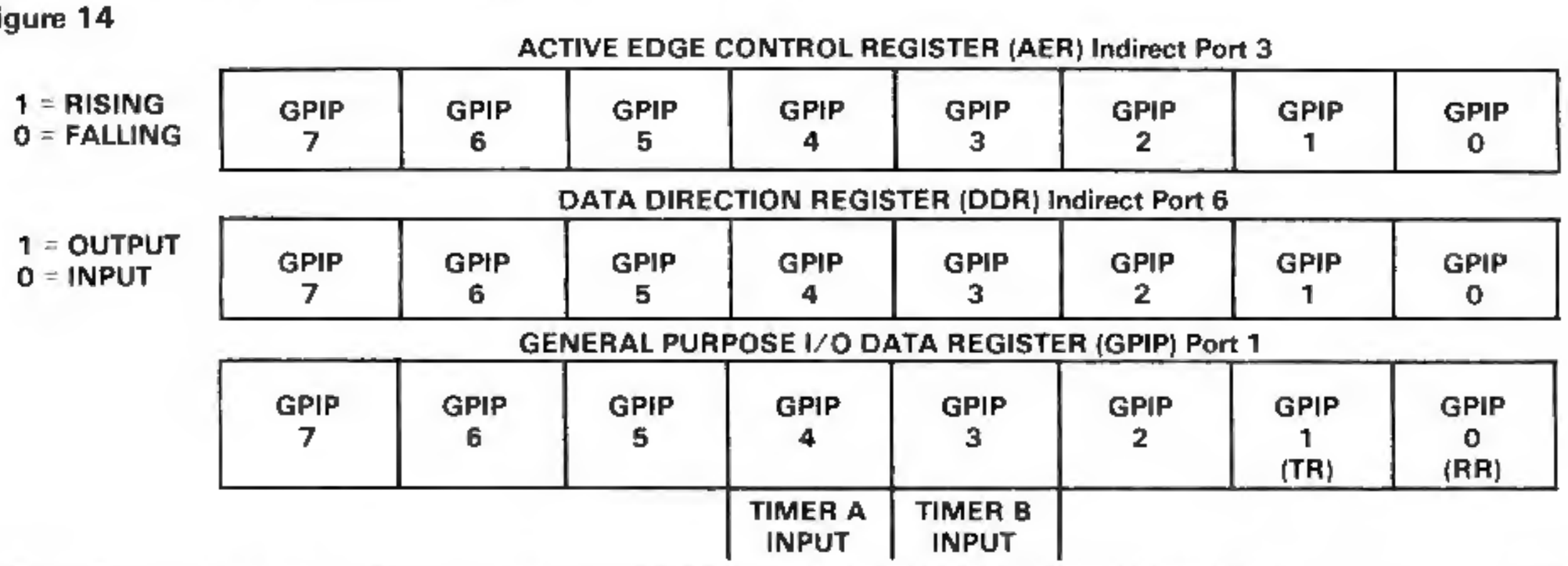
*Connects transmitter output to receiver input. In loopback mode, transmitter goes high when disabled. Also connects clocks with TC given priority.

USART DATA REGISTER (UDR) Port F

Figure 13

GENERAL PURPOSE I/O CONTROL REGISTERS

Figure 14



interrupts (Port 5, Indirect) for the desired channel (Receive error or Transmit error) and by masking these bits off (Port 7). Once the transfer is complete, the Interrupt Pending Register (Port 3) can be polled to determine the presence of a pending error interrupt, and therefore an error.

GENERAL PURPOSE I/O - INTERRUPT PORT

The General Purpose I/O - Interrupt Port provides eight I/O lines that may be operated either as inputs or outputs under software control. In addition, each line may generate an interrupt on either a positive going edge or a negative going edge of the input signal.

Two of the lines in this port provide auxiliary input functions for the timers in the pulse width measurement mode and the event counter mode. Two others serve as auxiliary output lines for the USART, one indicating the Receive Buffer Full condition (RR) and the other indicating the Transmitter Buffer Empty condition (TR). These may be used as handshake signals for a DMA controller or other external control circuitry.

GENERAL PURPOSE I/O CONTROL REGISTERS

The General Purpose I/O and Interrupt Port has 2 control registers. One allows the programmer to specify the Active Edge for each bit that will trigger the interrupt associated with that bit. The other register specifies the Data Direction (input and output) associated with each bit. The third register is the actual data I/O register used to input or output data to the port. When the USART is programmed to use DMA signals, this overrides the GPIP data and the DDR. The General Purpose I/O Control and Data Registers are illustrated in Figure 14.

MK3801 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... –25°C to + 100°C
Storage Temperature ..... –65°C to + 150°C
Voltage on Any Pin with Respect to Ground ..... – 3 V to + 7 V
Power Dissipation ..... 1.5 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5% unless otherwise specified.

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{IH}	Input High Voltage	2.0	V_{CC} + .3	V	
V_{IL}	Input Low Voltage	–0.3	0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –120 μA
V_{OL}	Output Low voltage		0.4	V	I_{OL} = 2.0 mA
I_{LL}	Power Supply Current		180	mA	Outputs Open
I_{LI}	Input Leakage Current		±10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT}=2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		–10	μA	V_{OUT} = 0.4 V

All voltages are referenced to ground.

CAPACITANCE

T_A = 25°C, f = 1 MHz unmeasured pins returned to ground.

SYM	PARAMETER	MAX	UNIT	TEST CONDITION
C_{IN}	Input Capacitance	10	pf	Unmeasured pins returned to ground
C_{OUT}	Tri-state Output Capacitance	10	pf	

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} – +5 V ± 5% unless otherwise noted.

SIGNAL	SYMBOL	PARAMETER	MK3801-0		MK3801-4		MK3801-6*		UNIT	CONDITION
			MIN	MAX	MIN	MAX				
A_0-A_3	T_{SAR} & T_{SAW}	Address setup time prior to falling edge of $\overline{CEWR}$ or $\overline{CERD}$	80		30				ns	
	T_{HAR} & T_{HAW}	Address hold time after rising edge of $\overline{CEWR}$ or $\overline{CERD}$	0		0				ns	
$\overline{CEWR}$	T_{WM}	$\overline{CEWR}$ pulse width low (write cycle)	360		205				ns	
	T_{WW}	$\overline{CEWR}$ high time between write cycles	580		400				ns	
	T_{WRD}	$\overline{CEWR}$ high to $\overline{CERD}$ low	580		400				ns	
$\overline{CERD}$	T_{RDL}	$\overline{CERD}$ pulse width low (read cycle)	400		250				ns	
	T_{RR}	$\overline{CERD}$ high time between read cycles	300		200				ns	
	T_{MIRD}	Rising $\overline{MIRD}$ to falling $\overline{MIRD}$	225		165				ns	
	T_{RDW}	$\overline{CERD}$ high to $\overline{CEWR}$ low	125		100					
$\overline{MI}$	T_{SMI}	$\overline{MI}$ setup time prior to falling $\overline{IORQ}$ during interrupt acknowledge	800		500				ns	
IORQ	T_{IOL}	$\overline{IORQ}$ low time	300		185				ns	
IEI	T_{SIEI}	Setup to falling $\overline{IORQ}$ during interrupt acknowledge	140		80				ns	
	T_{SRD}	Setup prior to end of 4D read on RETI	100		50				ns	
D_0-D_7	T_{SDMI}	Data valid prior to rising $\overline{RD}$ ($\overline{MI}$ cycle)	50		50				ns	Load 100 pf +
	T_{HDMI}	Data hold time after rising $\overline{RD}$ ($\overline{MI}$ cycle)	0		0				ns	1 TTL load
	T_{DRD}	Data output delay from $\overline{CERD}$		400		250			ns	
	T_{SDW}	Data setup time to rising edge of $\overline{CEWR}$	350		280				ns	
	T_{HDW}	Data hold time from rising edge of $\overline{CEWR}$	0		0				ns	
	T_{DDI}	Data output delay from falling $\overline{IORQ}$ during interrupt acknowledge		320		185			ns	

*To be determined

A.C. CHARACTERISTICS (Continued)

SIGNAL	SYMBOL	PARAMETER	MK3801-0		MK3801-4		MK3801-6*		UNIT	CONDITION
			MIN	MAX	MIN	MAX				
	T_{DHVZ}	Data hold time following $\overline{M1}$ $\overline{IORQ}$ during interrupt acknowledge cycle	0		0				ns	
	T_{DDZ}	Delay to float		150		100			ns	
I_0-I_7	T_{IPW}	Minimum active pulse width	200		100				ns	
	T_{ICY}	Minimum time between active edges	200		100				ns	
	T_{DIW}	Data valid from rising $\overline{CEWR}$		600		500			ns	Load 100 pf +
RR	T_{DRR}	Delay from rising RC		360		240			ns	1 TTL load
TR	T_{DTR}	Delay from rising TC		450		295			ns	
TAO-TDO	T_{DTR}	Timer output low from rising edge of $\overline{CEWR}$ (A & B) (Reset T_{OUT})		600		500			ns	Load 100 pf +
	T_{DTI}	T_{OUT} valid from Internal timeout		$2\ t_{CLK}$ +400		$2\ t_{CLK}$ +300			ns	1 TTL load
TCLK	$T_{t_{CLKL}}$	Low time	130		90				ns	
	$T_{t_{CLKH}}$	High time	130		90				ns	
	$T_{t_{CKC}}$	Cycle time	300	2500	200	2500			ns	
RESET	T_{RSL}	Low time for part reset	3		2				μs	
IEO	T_{DIEOH}	IEO delay from rising edge of IEI		200		130			ns	Load 100 pf +
	T_{DIEOL}	IEO delay from falling edge of IEI		200		130			ns	1 TTL load
	T_{DIEOM}	IEO delay from falling edge of $\overline{M1}$ (interrupt occurring just prior to $\overline{M1}$)		270		190			ns	
	T_{DIEOA}	Delay to rising IEO from rising $\overline{IORQ}$ during interrupt acknowledge		1000		800			ns	
	T_{DIEOR}	Delay to rising IEO from rising edge of RD during ED fetch of RETI		500		400			ns	
INT	T_{DIX}	Delay to falling $\overline{INT}$ from external interrupt active transition		550		380			ns	Open drain load 100 pf + 2 1 K resistor

*To be determined

A.C. CHARACTERISTICS (Continued)

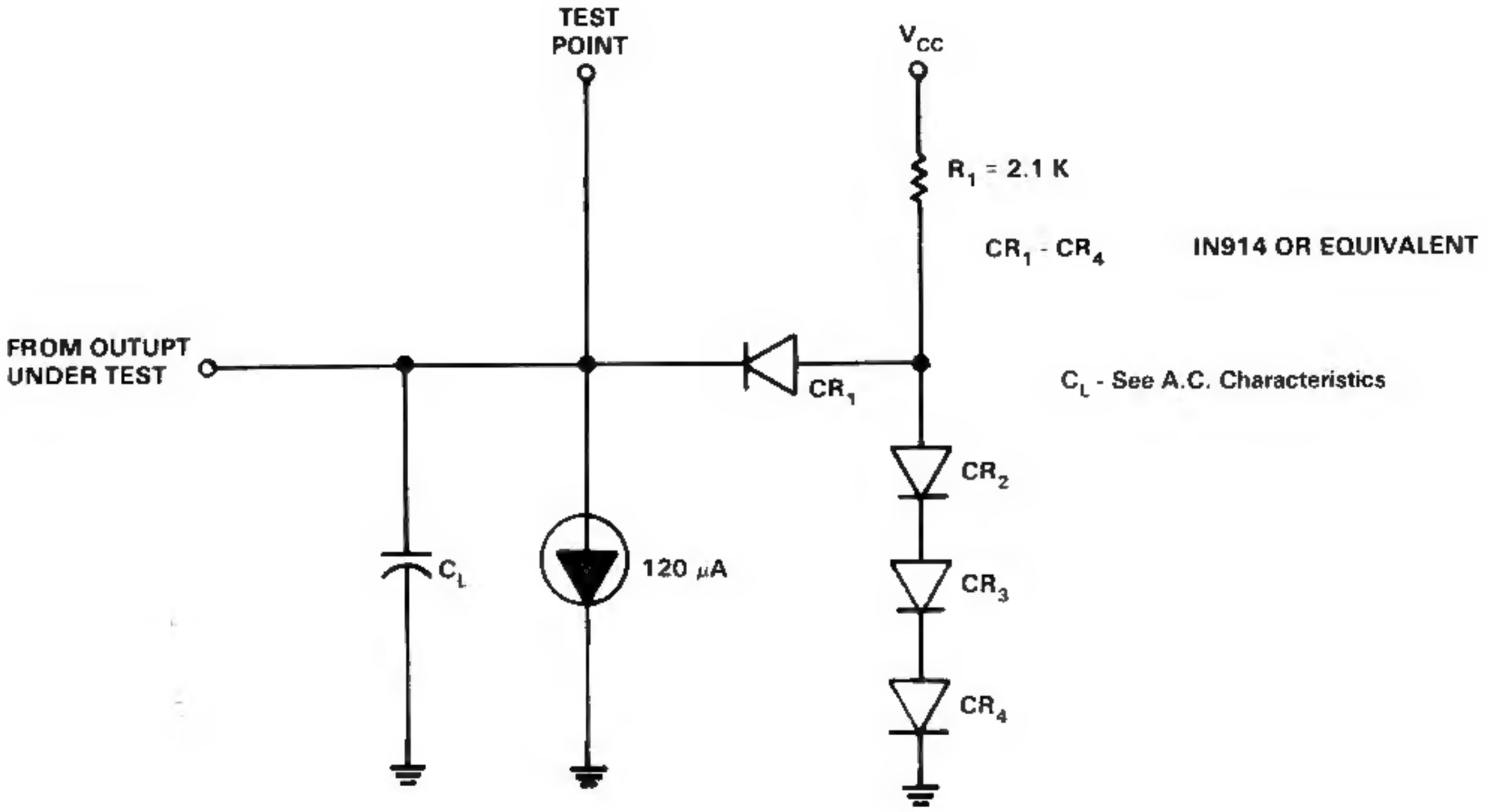
SIGNAL	SYMBOL	PARAMETER	MK3801-0		MK3801-4		MK3801-6*		UNIT	CONDITION
			MIN	MAX	MIN	MAX				
	T_{DII}	Delay to falling INT from internal interrupt transition		360		280			ns	
	T_{DTI}	Transmitter Internal interrupt transition delay from rising edge of TC		560		390			ns	
	T_{DRI}	Receiver buffer full internal interrupt transition delay from rising edge of RC		400		300			ns	
	T_{DREI}	Receiver error internal interrupt transition delay from falling edge of RC		550		340			ns	
SI	T_{SSI}	Serial in set up time to rising edge of RC (Divide by one only)	20		0				ns	
	T_{HSI}	Data hold time from rising edge of RC (Divide by one only)	400		350				ns	
SO	T_{DSO}	Data valid from falling edge of TC		420		390			ns	100 pf + 1 TTL load
TC	T_{TCL}	Low time	650		400				ns	
	T_{TCH}	High time	650		400				ns	
	T_{TCCY}	Cycle time	1.5		1				μs	
RC	T_{RCL}	Low time	650		400				ns	
	T_{RCH}	High time	650		400				ns	
	T_{RCCY}	Cycle time	1.5		1				μs	

*To be determined

NOTE: All A.C. measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (0.8 V), or V_{OH} (2.0 V).

OUTPUT LOAD CIRCUIT

Figure 15



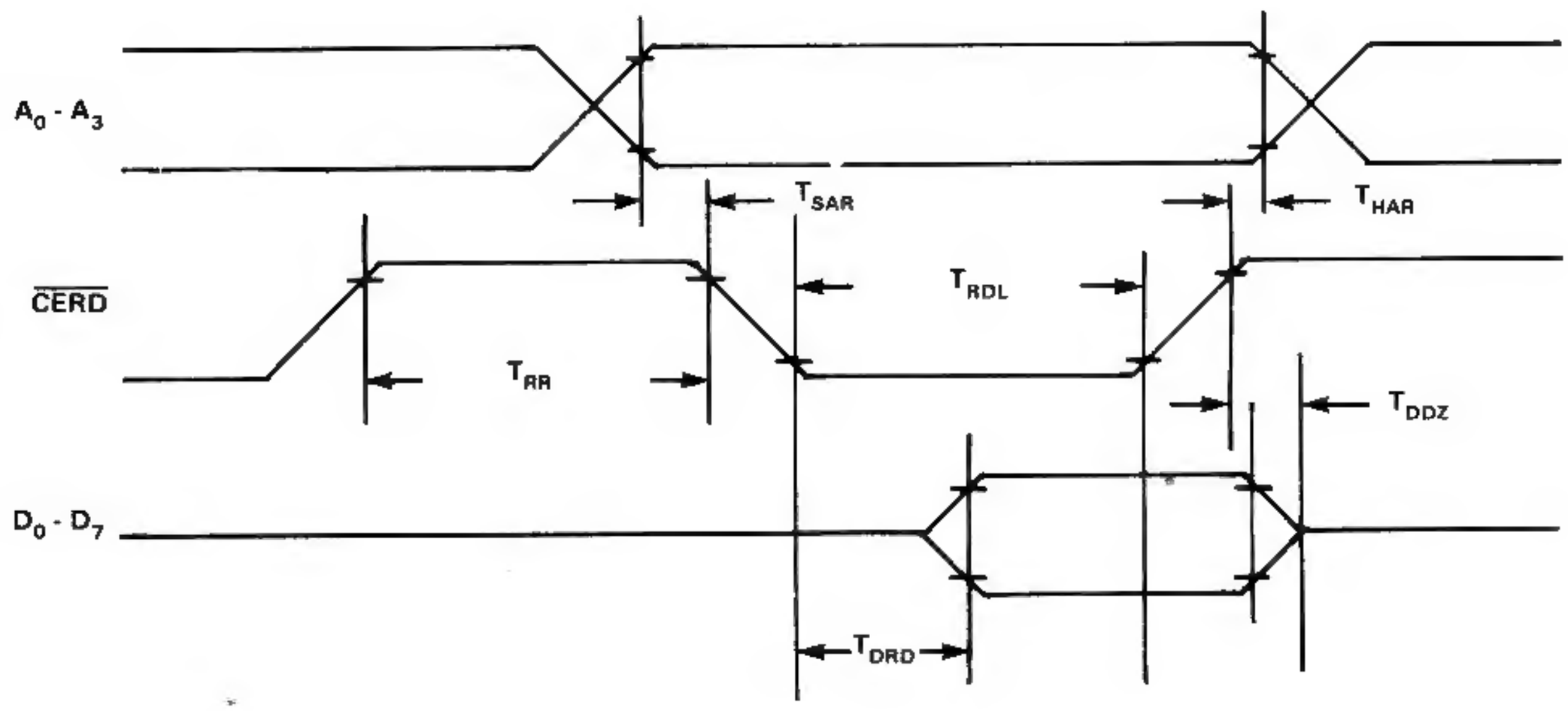
TIMING DIAGRAMS

Figure 16

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"		"0"
OUTPUT	2.0 V		0.8 V
INPUT	2.0 V		0.8 V
FLOAT	Δ V	=	0.5 V

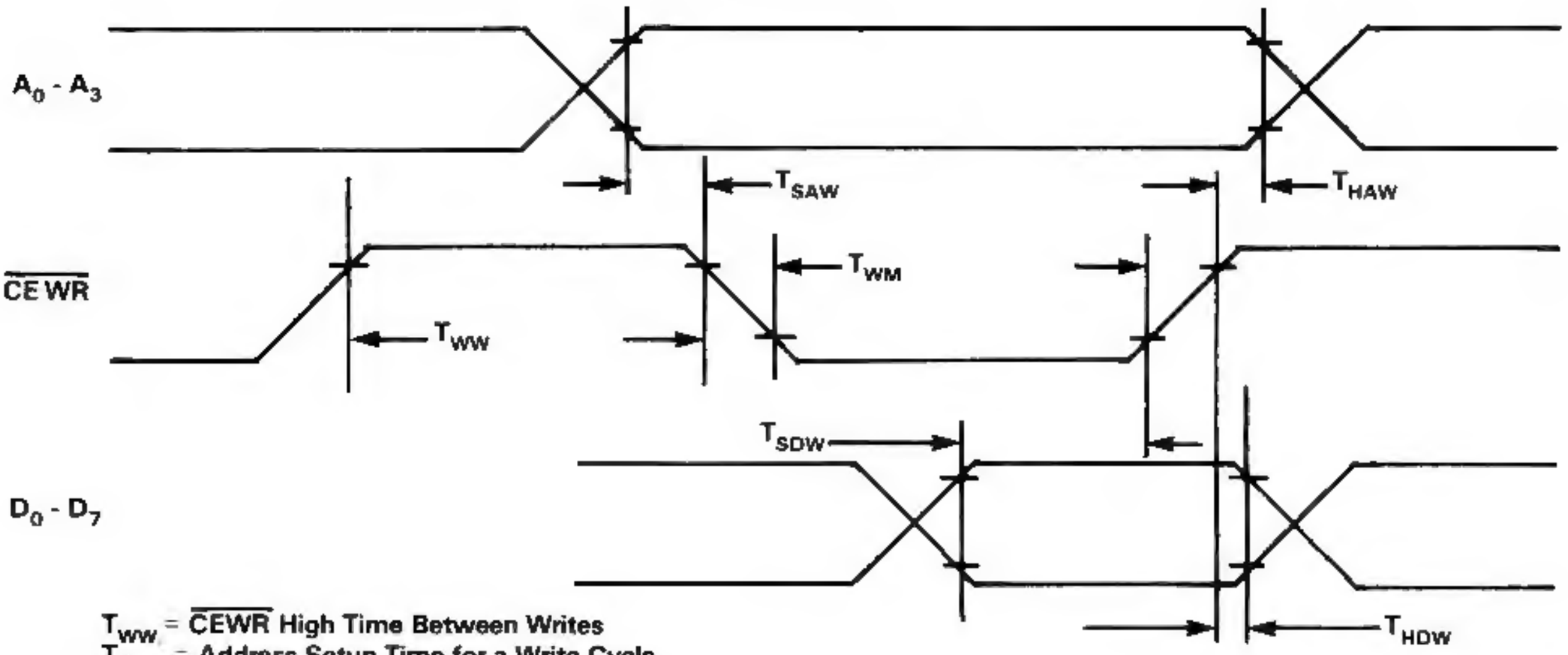
READ CYCLE



T_{SAR} = Address Setup Time for a Read Cycle
T_{DRD} = Data Output Delay from $\overline{CERD}$
T_{DDZ} = Time to Tri-State Following a Read Cycle
T_{HAR} = Required Address Hold Time Following a Read Cycle

WRITE CYCLE

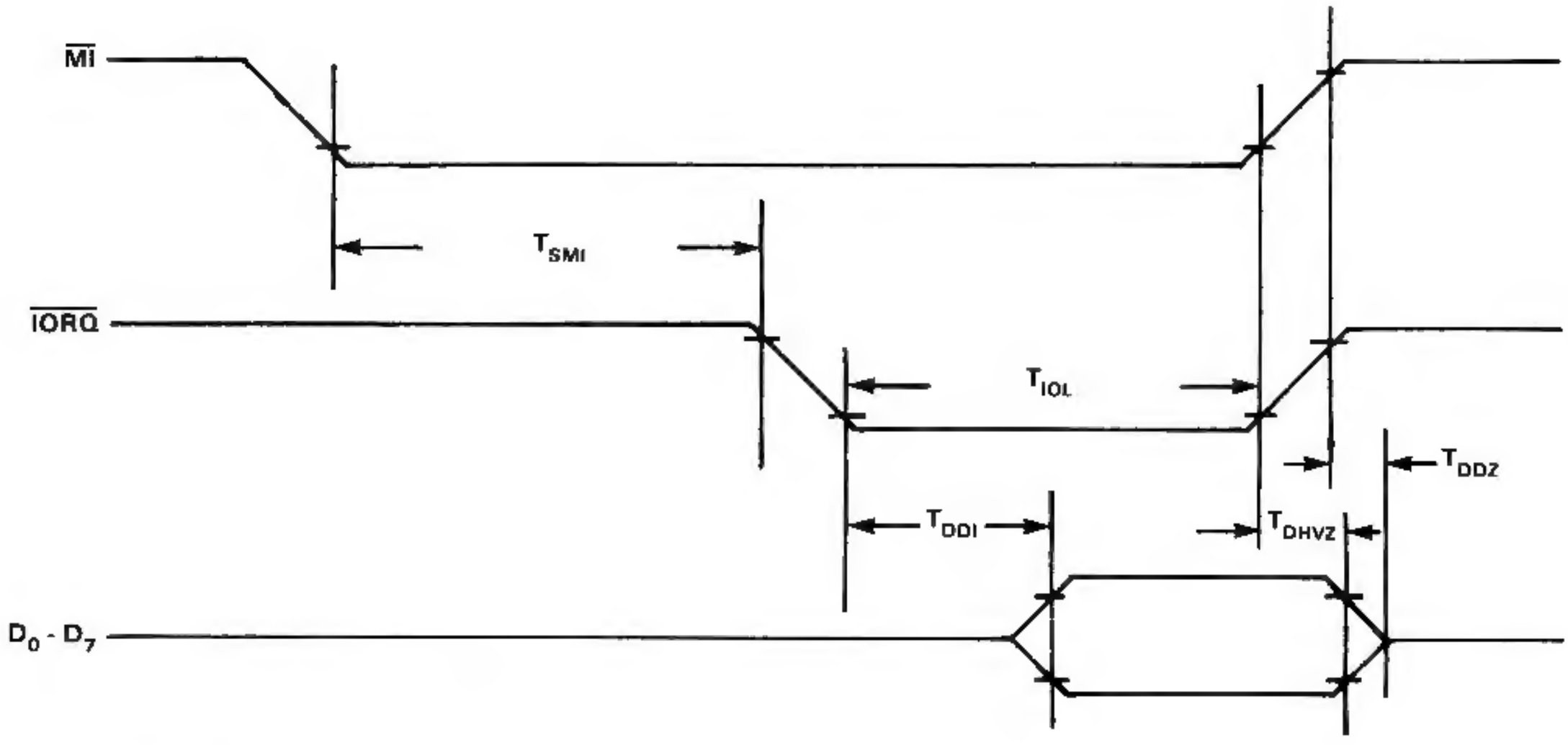
Figure 17



T_{WW} = $\overline{CEWR}$ High Time Between Writes
T_{SAW} = Address Setup Time for a Write Cycle
T_{SDW} = Data Setup Time Prior to the End of a Write Cycle
T_{HDW} = Required Data Hold Time Following a Write Cycle
T_{HAW} = Required Address Hold Time Following a Write Cycle
T_{WM} = $\overline{CEWR}$ pulse width low

INTERRUPT ACKNOWLEDGE CYCLE

Figure 18



T_{IOL} = $\overline{IORQ}$ Pulse Width Low
T_{SMI} = $\overline{M1}$ Setup Time prior to $\overline{IORQ}$ For an Acknowledge cycle
T_{DDI} = Access Time for Vector
T_{DDZ} = Time to Tri-State Following a Vector
T_{DHVZ} = Data hold time following $\overline{M1}$ $\overline{IORQ}$ during interrupt acknowledge cycle

TIMER A.C. CHARACTERISTICS

Definitions:

Error = Indicated Time Value - Actual Time Value

tpsc = t_{CLK} x Prescale Value

Internal Timer Mode

Single Interval Error (free running) (Note 2)	± 100 ns
Cumulative Internal Error	0
Error Between Two Timer Reads	± (tpsc + 4 t_{CLK})
Start Timer to Stop Timer Error	2 t_{CLK} + 100 ns to –(tpsc + 6t_{CLK} + 100 ns)
Start Timer to Read Timer Error	0 to –(tpsc + 6 t_{CLK} + 400 ns)
Start Timer to Interrupt Request Error (Note 3)	–2 t_{CLK} to –(4t_{CLK} +800 ns)

Pulse Width Measurement Mode

Measurement Accuracy (Note 1)	2 t_{CLK} to –(tpsc + 4t_{CLK})
Minimum Pulse Width	4t_{CLK}

Event Counter Mode

Minimum Active Time of I_3, I_4	4t_{CLK}
Minimum Inactive Time of I_3, I_4	4t_{CLK}

NOTES:

1. Error may be cumulative if repetitively performed.
2. Error with respect to T_{OUT} or INT if note 3 is true.
3. Assuming it is possible for the timer to make an interrupt request immediately.

ORDERING INFORMATION

PART NO.	DESIGNATOR	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3801N-0	Z80-STI	Plastic	2.5 MHz	0 to 70°C
MK3801N-4	Z80-STI	Plastic	4.0 MHz	0 to 70°C
MK3801N-6	Z80-STI	Plastic	6.0 MHz	0 to 70°C

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